HITACHI Analog·Hybrid Computer

Technical Information Series No.2

Information on Hybrid Interface

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CONTENTS

1.	General Description	1	
2.	Functions	2	
3.	Interface	2	
4.	Input/Output Requirements	4	
5.	Performance Specifications	4	

1. General Description

This literature provides the user or the hybrid-linkage maker with necessary, detailed information about linking the HITACHI-505 (hereinafter called 505) and a digital computer so as to compose a complete hybrid computing system.

The detailed information descrived in the literature includes the interface requirements for transfer of input and output signals between 505 and the hybrid linkage, the maximum available number of channels, as well as reference specifications of equipment to be included in the linkage. Since the requirement for interface hardware between the hybrid linkage and a specific digital computer varies according to I/O channel provisions of the available digital computer, this literature mainly deals with the basic and general interface requirements.

This literature serves as one of the volumes in the information series, which provides necessary information for adapting the HITACHI-505 to a hybrid computing system.

2. Functions

In order to compose a hybrid computing system by linking 505 and any particular digital computer (hereinafter called D-C), the hybrid linkage shall be provided with the following functions:

(1) Transfer of data between 505 and D-C.

The linkage should be capable of transfering data at high speed and high accuracy with the aids of such functions as A-D conversion, D-A conversion, scanning, distributing.

- (2) Automatic Setting of Initial condition of Integrator and Function generations in 505 D-C should be provided with the control function to control the setting of servo-set potentiometers (SP) and servo-set function generators (SFG).
- (3) Operation Mode Control of 505

D-C should be able to select the operation mode of 505 by means of its specific control signals.

(4) Mutual Control between 505 and D-C

The operating signals generated on the 505's patch panel and operating program proceeded on D-C can be interconnected through the general purpose control signals (Ci) and (Co) that are transmitted from 505 to D-C and vice versa respectively, so that the mutual control between 505 and D-C will effected.

(5) Synchronized Operation between 505 and D-C

The procedure of the operating program of D-C should be able to be synchronized with the operation of 505.

(6) Output Readout of 505's DC Amplifiers

By adding and making use of the automatic output selector (OPTION), individual output*1 of DC amplifiers should be able to addressed and read out by the digital voltmeter or the A-D converter.

*1: See para. 6, Reference (1) and also para. 2-(4).

(7) Control of Recorders

Provision should be made that D-C is able to control chart-driving and up-down

movement of the writing pen for the strip-chart recorder as well as for the XY recorder, by means of its specific control signals.

(8) Interrupt Control

D-C should have the function to accept such program interruption by two, which the program being proceeded on D-C can be interrupted.

3. Interface

3.1. Signals to be transferred between 505 and the linkage.

Specifications of the input and output signals transferred between 505 and the linkage shall be shown on the following Table:

The linkage shall be provided with a buffer section in order to match input and output levels. The buffer section is to convert the input signals into the necessary signals and levels to fit operation on the linkage, and also converts the output signals into the necessary signals and levels to match with operation on 505.

(1) Output Signals sent from 505 are specified as follows.

SIII IIII W	T4	Name of Signal	Туре	Output Voltage		Rise	Max. Allow-	Max. Allow-	
Vasaua	Item #			OFF	ON	Time	able Load Current	able Load Capacitance	
ing,	nnsoil ,no	Analog Data	Analog Voltage	±100V	Range	it dane	10mA	0.001 µF	
606 nt s	2 noDereney a lo weltte	General Purpose Control (Ci) (include SP and/o	emetel to	±0.5V	+5V +8V	10 μS or less	1mA	0.001 µF	
	3	Digital Volt- meter	dance w		Manual for the Digital				
cific	4	Clock	Step	±0.5V	+5V +8V	1μS or less	1mA	0.001 µF	
	5	Mode Sense (RESET COMPUTE)	Step	±0.5V	+5V +8V	10µS or less	10mA	0.001 µF	
ol signals	oose contr	Interlock ago but least data and farency set do and vice very	Make/ Break of Relay Contact	rconnect tted from	+24V	ignals -C can st are t	10mA		

NOTE: The specifications listed above will apply to the 505 modified for adapting it to a hybrid computing system.

The procedure of the operating program of D-C should be able to be synchronized

(2) Control and data signals sent from the linkage shall meet following specifications.

	N of Simol	Type	Output Voltage		Rise	Max. Allow- able	Max. Allowable Load	
Item #	Name of Signal	Signal	OFF	ON	Time	Load Current	Capacitance	
1	Analog Data	Analog Voltage	±10V or ±100V	pamining or		10mA	0.001 μF	
2	General Purpose Control (Co)	Step	±0.5V	+7V	10 μS or less	5mA		
3	Recorder Control	In accor	rdance v	vith Ins.	Manua	al for Rec	order.	
4	Operation Mode Control	General Pargose Control Signal (Co) Max. F						
O-1 Multiple	RESET, COMPUTE, HOLD	Pulse width; 1ms or longer	±0.5V	+5V~ +8V	10 μS or less	5mA	0.001 μF	
5	POTSET, ALL RESET	Pulse width; 10ms or longer	±0.5V	+5V~ +8V	10 µS or less	5mA	0.001 μF	
	REP OPE	Step	±0.5V	+5V~ +8V	10 µS or less	5mA	0.001 μF	
6	SP, SFG all kind of Signal	Step	±0.5V	+5V~ +8V	10 μS or less	5mA	0.001 μF	

(3) Transfer of signals between the linkage and D-C goes through the interface section. The interface section must be prepared in accordance with the available function of D-C.

The principal functions provided by the interface section, in conjunction with operations of the linkage shall be as follows:

The interface section:

- 1 receives data signals from D-C and separates them into data and address portions, and further separates the address portion into "READ" and "WRITE" portions, which will be sent to the appropriate operating elements in the linkage.
- 2 receives and reads input data from the linkage, and transfers them to D-C.
- (3) keeps sending the "BUSY" signal to D-C while the linkage is being operated by the instruction from D-C, or while the linkage is the interlock signal "ON", and releases the "BUSY" condition upon receipt of the "END" signal or the interlock signal "OFF" from the linkage so that transmission of the succeeding operating instruction from D-C may become possible.
- (4) transfers the interrupt signal from the linkage to D-C.
- (5) Date signal transmission between the linkage and the interface shall be proceeded in the pattern of 12 bits (or 16 bits) parallel code at each one time.

4. Input/Output Requirements

(1)	Analog Input	Max.	8 CH.						
(2)	Digital Input								
	and the same				mest				
	General Purpose Control Signal (Ci) Digital Voltmeter Output Readout	Max.	6 CH. 1 CH.						
	Clock Mode Sense (RESET, COMPUTE) Interlock		2 CH. 1 CH. 1 CH.	Ansing Da					
	Interiock		1 CII.						
(3)	Analog Output	Max.	8 CH.						
(4)	Digital Output								
	General Purpose Control Signal (Co)	Max.	6 CH.	mod revised for mod a blosvine					
	Recorder Control (Paper Feeding & Pen-Up/Down Movement)								
	Strip-Chart Recorder X-Y Recorder		1 CH. 1 CH.	HOLD					
	Operation Mode Control	olibiw							
	RESET		1 CH.						
	COMPUTE		1 CH.						
	HOLD AND HOLD		1 CH.						
	POT SET		1 CH.						
	ALL RESET		1 CH.						
Hay	REP OPE		1 CH.						
	SP/SFG Setting Output								
	For addressing SP		1 CH.						
	For addressing SFG								
	Setting Signal		1 CH.						

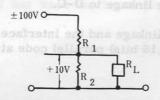
Note: SP stands for Servo-set Potentiometer SFG stands for Servo-set Function Generator

The number of sets that can be addressed depends on the specific configuration of the HITACHI-505, which is capable of designating 72 sets of SP and 2 sets of SFG at its maximum.

5. Performance Specifications

5.1. Analog Input

The $\pm 100 \mathrm{V}$ range analog input voltage, which is the output of the 505's amplifier, shall be divided by a voltage divider and reduced to a suitable voltage ($\pm 10 \mathrm{V}$ or $\pm 5 \mathrm{V}$) which will be applied to the A-D converter through the multiplexer. The input resistance of the voltage divider shall be more than 10 kilo-ohms. Note that the input resistance parameter (R_{AD}) should be determined with consideration for the load (the input resistance to the multiplexer) to be connected in parallel with the voltage divider.



Voltage Dividing Ratio

$$R_{AD} = \frac{1}{10} = \frac{R_2//R_L}{R_1 + R_2//R_L}$$

where: R_L = Load Resistance

$$R_2 / / R_L = \frac{R_2 R_2}{R_2 + R_L}$$

Specifications of equipment shall be as follows: (Performance of the equipment should meet the following specifications.)

(1) Multiplexer

Input Voltage Range: ±10V (or ±5V) Number of Channels: Channel Selection:

Up to 8 channels Addressable

(Any channel may be selected by the D-C's

program).

±0.1% of full scale 10V (or 5V) Accuracy:

(2) A-D Converter

Input Voltage Range ±10V (or ±5V) Conversion Rate Accuracy

5 KC

0.1% ±1/2 LSD (Least Significant Digit)

Output Code Sign + Binary 10 bits

(3) Multiplexer Control

The Multiplexer Control should be provided with functions to control the switching of the multiplexer when addressed, to cause the A-D converter to start its operation and to send the END signal to the interface section after the completion of the operation has been confirmed.

In other words, the instruction from D-C will cause the interface section to read the analog input data and transfer it to D-C.

5.2. Digital Input

(1) General Purpose Control Signal (Ci)

The logical output of 505 shall be taken out as input to D-C. The control signal for each channel shall correspond to a bit in the pattern of the input signal for D-C. The "ON" or "OFF" of each channel shall be represented by the respective bit's "ON" or "OFF" in the pattern. Since the total number of channels is six, the pattern consists of six bits, which are handled as one group in transferring. The digital input, thus grouped, are read by D-C, one group at a time, upon issuance of the "SENSE" instruction from D-C.

Note that whenever any bit of the six bits in a digital input pattern changes from "OFF" to "ON", it is required that the linkage is to send a request for the "SENSE" signal to D-C so that the new pattern can be read out by D-C.

(2) Digital Voltmeter Output Readout

The output of digital voltmeter is to be applied to the linkage as its input, and the signal level shall be adjusted by the buffer section.

When the word structure of the digital voltmeter output is in the form of sign + BCD (Binary Coded Decimal) 4 digits (or 5 digits), the total number of bits required is 20 bits (or 24 bits). Thus, the voltmeter output should be read in two times and then transferred to D-C. Since data is expressed in the fixed point system, it is not necessary to read the decimal point. When a digital voltmeter is addressed, the digital voltmeter control drives the voltmeter to the "single scan" mode of operation.

Upon completion of the conversion, the interface section receives END signal from the digital voltmeter and transfers it to the interface section so that the conversion data can be read by D-C.

(3) Control Input Signal Secretary and the secretary to second secretary to second sec

For Control input signal to D-C three types of Control input signal are required; Ci, CLOCK, and MODE SENSE.

The Ci signal can express six conditions, as described in subpara. (1), while the CLOCK signal expresses two, and the MODE SENSE signal does two or RESET and COMPUTE.

A provision must be made that, whenever a condition is turned from "OFF" to "ON", a request for the SENSE signal is generated. Also, it is necessary that these conditions can be read by issuing the SENSE signal directly from D-C by means of its operating program.

(4) Interlock

While the patch panel of 505 is in "DISENGAGE" condition, the INTERLOCK signal is being sent out. During this period, it is necessary that the interface section keeps sending the "BUSY" signal to D-C and that the data transfer is halted.

5.3. Analog Output

The specifications of the D-A converter shall be as follows:

(Performance of the equipment should meet the following specifications.)

Output Voltage Range \pm 10 VOutput Current \pm 5 mAConversion Rate5 KC or above

Accuracy $\pm 0.1\% \pm 1/2$ LSD of full scale Input Code Sign + Binary 10 bits (or 11 bits)

Number of Channels

Channel Selector Addressable (To be addressed by D-C's program)

The D-A converter does not provide setting date channel itself, but D-C does.

5. 4. Digital Output

(1) General Purpose Control Signal (Co)

The general purpose control signal shall be issued from D-C and shall control the logical operation of 505. The control signal for each channel is to correspond to each one bit of the D-C output. Since the number of channels is six altogether, the pattern of (Co) consist of 6 bits and shall be handled as one group at each time in transferring. All of 6 bits in each group shall be set into the register by instruction of D-C. It is also necessary that these signals are sent to the patch panel of 505 through GRUNKS TR-151. When the bits that are sent from D-C to the register become "OFF", these output signals also become "OFF".

(2) Recorder Control

Each of the following channels is to correspond to 4 bits of the D-C output.

Strip-Chart Recorder: 1 CH Paper Feeding Start/Stop
Pen-Up/Down Movement
X-Y Recorder : 1 CH Paper Feeding Start/Stop
Pen-Up/Down Movement

In contrast to the Co signal which must be sent to the patch panel of 505, as stated in the previous subparagraph, these recorder control signals shall be sent from the linkage to the recorder without going through the 505 unit. The linkage shall be provided with a register to store the 4 bits of each setting signal.

(3) Operation Mode Control and the major and all nothing to half dead

Signals which control the operation mode of 505 shall be issued from D-C. Six types of control signal are available as listed below: These signals are required to be transmitted to 505 in three different waveforms.

RESET 1 ms pulse width

COMPUTE Same as above.

HOLD Same as above.

POT SET 10 ms pulse width.

ALL RESET Same as above.

REP OPE Step Signal

Each of the above signals consists of 1 bit and therefore, 6 bits altogether shall be handled as one group at a time.

It should be noted that only one bit out of the six bits is permitted to become "ON" at a time because 505 does not take more than two modes at the same time.

(4) SP Setting Output

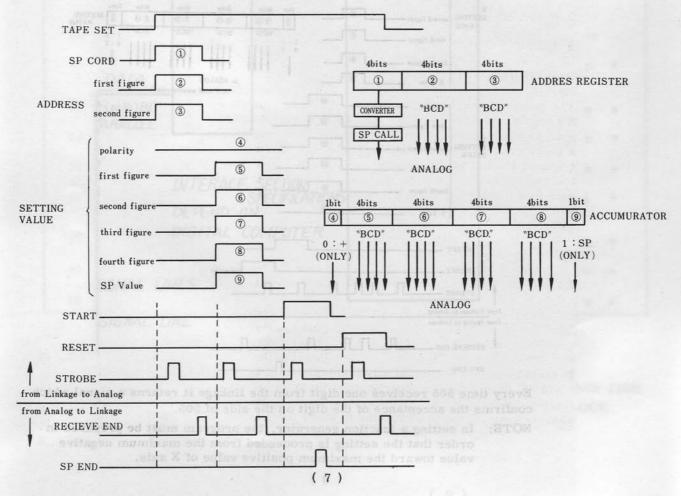
The setting of servo-set potentiometers of 505 should be performed in the following manner.

The procedure is:

- (i) Special "Co" signal which means that the setting of servo-set potentiometers is going to be on prosedure shall be send from the linkage to 505 by the instruction of the operating program of D-C.
- (ii) The signals which represent the potentiometer number and the setting values shall be sent from the linkage to 505, one after another in the BCD code (4 bits) in the following sequence.

This sequence is controlled by instructions of D-C.

SP SET SEQUENCE



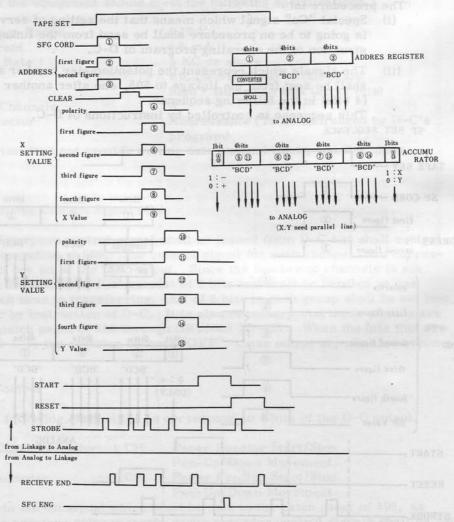
Each digit or position is in the form of the BCD code. Everytime 505 receives one digit from the linkage, it returns a signal to the linkage which confirms the acceptance of the digit on the side of 505. In succession, the linkage sends the END signal to the interface section.

NOTE: On procedure of setting a SP to a value, polarity of the value in the program must be properly set to positive in advance.

(5) SFG Setting Output

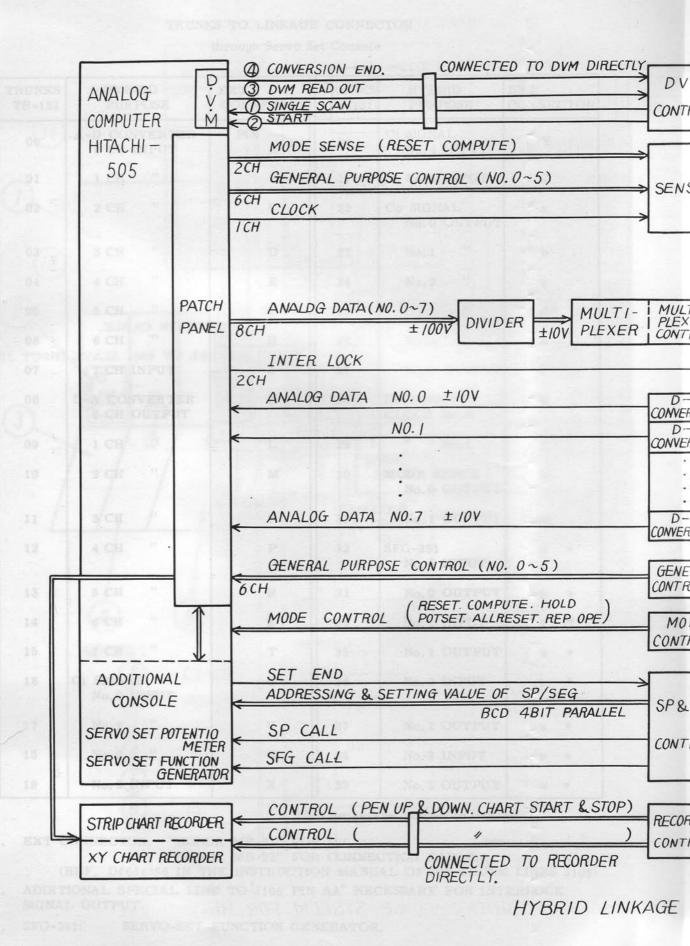
The setting of servo-set function generators of 505 shall be performed by the operating program of D-C in the following manner. The specifications of the control signal to drive a SFG are the same as those for a SP. The setting procedure is as follows:

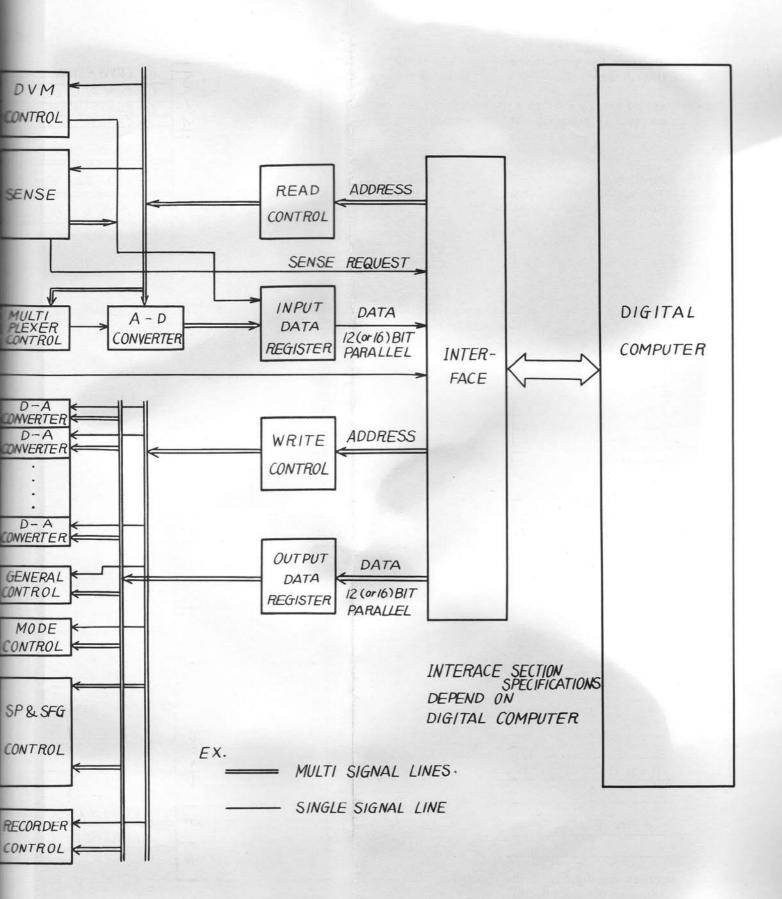
- i) Specific "Co" signal which means that the setting of a Servo-set function generator is going to be on procedure shall be sent from the linkage to 505 by the instruction of D-C program.
- ii) By proceeding the program, the signals which represent the function generator number and setting value of X and Y acid shall be sent from the linkage to 505, one after another in the BCD code (4 bits), in the following sequence.



Every time 505 receives one digit from the linkage it returns a signal which confirms the acceptance of the digit on the side of 505.

NOTE: In setting a function generator, the program must be prepared in order that the setting is proceeded from the maximum negative value toward the maximum positive value of X axis.





GE SYSTEM FOR HITACHI 505

TRUNKS TO LINKAGE CONNECTOR

through Servo Set Console

TRUNKS TR-151	HYBRID PURPOSE	EXT CONNECTOR	TRUNKS TR-151	HYBRID PUR POSE	EXT CONNECTOR
00	A-D CONVERTER 0 CH INPUT	PIN A	20	Ci SIGNAL No. 4 INPUT	Y
01	1 CH "	В	21	No.5 INPUT	Z
02	2 CH "	С	22	Co SIGNAL No.0 OUTPUT	a ()
03	3 CH "	D	23	No.1 "	b
04	4 CH "	Е	24	No. 2 "	С
05	5 CH "	F	25	No. 3	da H
06	6 CH "	Н	26	No. 4 "	e
07	7 CH INPUT	J	27	No.5 OUTPUT	f
08	D-A CONVERTER 0 CH OUTPUT	K	28	INTERRUPT CLOCK No.0	h
09	1 CH "	L	29	" No.1	(2)(3)
10	2 CH "	М	30	MODE SENCE No.0 OUTPUT	k
11	3 CH "	N	31	No.1 OUTPUT	m
12	4 CH "	Р	32	SFG-251 No. 0 INPUT	n *
13	5 CH "	R	33	No.0 OUTPUT	p *
14	6 CH ''	S	34	No.1 INPUT	r *
15	7 CH ''	T A	35	No.1 OUTPUT	s *
16	Ci SIGNAL No.0 INPUT	U	36	No.2 INPUT	t *
17	No. 1 "	v	37	No. 2 OUTPUT	u *
18	No. 2 "	w	38	No.3 INPUT	v *
19	No.3 INPUT	x	39	No.3 OUTPUT	w *

* Not necessary connect to linkage

1. EXT CONNECTOR: "HONDA MB-21" FOR 505.
"HONDA MB-22" FOR CONNECTION CABLE
(REF. D#634396 IN THE INSTRUCTION MANUAL OF 505 TRUNK LINES J105)

- 2. ADDITIONAL SPECIAL LINE TO "J105 PIN AA" NECESSARY FOR INTERLOCK SIGNAL OUTPUT.
- 3. SFG-251: SERVO-SET FUNCTION GENERATOR.

MODE CONTROL TO LINKAGE CONNECTOR

	MODE CONTROL	EXT CONNECTOR		
	RESET INPUT	AOMEC	HYBRID PURPOSE	
	COMPUTE INPUT	ин в нат	A-D CONVEN	
	HOLD "	C	HD I	
	POT SET "	D	0 H2 S	
arro.	ALL RESET " REP OPE "	E	" HOE	
	REP OPE "	F .	H. H. C.	

1. EXT CONNECTOR; "HONDA MB-5" FOR 505.
"HONDA MB-6" FOR CONNECTION CABLE.

(REF. D#634396 IN THE INSTRUCTION MANUAL OF 505. SLAVE INPUT J8.

No.5 OUTPUT			
		3 CH "	
No.1 INPUT			
	- 88		
	88		

DRITIONAL SPECIAL LINE TO JIES PIN AA' NECES ENAL OUTPUT,

(11)

